REMARKS

Claims 1-14 are presented for further examination. Claims 1 and 5-14 have been amended.

In the Office Action mailed October 1, 2004, the Examiner objected to claim 1 because of informalities therein. Applicant has adopted the Examiner's suggestion and amended claim 1 to include the indefinite article "an" before "input."

Claims 1, 3, and 4 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,710,960 ("Sato"). Claim 2 was rejected as obvious under 35 U.S.C. § 103(a) over Sato in view of applicant's admitted prior art in Figures 1-4. Claims 5-14 were found to be allowable.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

An improved binary decoder is provided that includes selection means for activating a selected output corresponding to an input binary value, and deselecting means coupled to each output that deactivates all other outputs when the selected output is activated. In one embodiment a circuit arrangement is provided having a single output connected to the selected output of the selection means and a plurality of outputs, each of which is connected to one of the remaining outputs of the selection means such that when the input of the circuit arrangement is active all the other outputs of the decoder are forced to the inactive state.

Sato, U.S. Patent No. 4,710,960, is directed to speech-adaptive predictive coding having reflected binary encoder/decoder. Sato describes an encoder that includes a delay circuit, quantizer, predictor coefficients residual power extractor, and reflected binary encoder that outputs digital signals to a multiplexer 6. Signals are transmitted from the multiplexer 6 in an encoded format to a demultiplexer 11, which then outputs the received bit sequence y1 into two sequences, a predicted residual bit sequence y2 and a parameter information bit sequence y3.

As Sato describes at column 4, lines 35-68, the predicted residual bit sequence y2 is amplified by an amplifier 12 to a gain (G) that is added to the output of a predictor circuit 13. The predictor circuit 13 receives at one input the parameter information bit sequence y3 when a

burst error detector 16 transmits a burst error detection signal y5. This is processed through a reflection binary code decoder 19 and predictor coefficients residual power restoring circuit 14 and predictor 13 for summation with the predicted residual bit sequence y2. The sum is then output through a digital-to-analog converter 15, which provides a demodulated speech output, selecting only one output and deselecting all other outputs. Rather, Sato teaches that both outputs can be used, depending on the condition of the burst error detector 16 output signal y5.

Turning to the claims, claim 1 is directed to an improved binary decoder that comprises a selection means for activating a selected output corresponding to an input binary value, and deselecting means coupled to each output that deactivates all other outputs when the selected output is activated. Nowhere does Sato teach or suggest such an improved binary decoder. Rather, the demultiplexer 11 of Sato merely provides two output sequences y2, y3. A burst error detector receives as input a signal y4 and outputs a burst error detector signal y5 to select either y5 or the second sequence y3 from the demultiplexer 11. Thus, Sato does not meet the recited combination in claim 1 because it does not deactivate all other outputs when a selected output is activated. More particularly, it does not deselect the output sequence y2 when the output sequence y3 is selected at the selector switch 18. In view of the foregoing, applicant respectfully submits that claim 1 as well as claims 2-4 are clearly allowable over Sato, taken alone or in any combination with the admitted prior art.

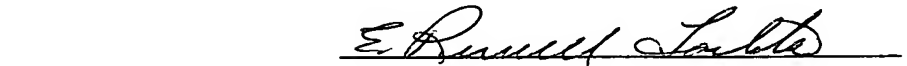
Claims 5-14 have been amended to correct typographical errors, and no new matter has been added. Claims 5-14 remain allowable.

In view of the foregoing, applicant submits all of the claims in this application are clearly in condition for allowance. In the event the Examiner disagrees or finds minor informalities, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application.

Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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